

**AMENDMENTS TO THE DRAWINGS**

The attached replacement sheet of drawings includes changes to Figure 5. This sheet, which includes Figs. 5-6, replaces the original sheet including Figs. 5-6. In Figure 5, the notation "Gate voltage capacity M1, M2, M3, M4 > Gate voltage capacity MN1, MN2, MP1, MP2" has been added. No new matter is added.

The attached new sheet of drawings includes new Figure 15. Figure 15 illustrates exemplary gate oxide thicknesses of transistors M1-M4 and transistors MP1, MP2, MN1, MN2 of Fig. 5, as disclosed in the specification as filed, at, for example, page 13, lines 22-26.

**REMARKS**

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

The Applicants appreciate the acknowledgement of allowable subject matter in claims 2, 7-14 and 18.

By the foregoing amendment, claims 2-9, 11-14 and 18-20 have been amended, and claims 1 and 17 have been canceled without prejudice or disclaimer for filing in a continuation application. Thus, claims 2-16 and 18-20 are currently pending in the application and subject to examination.

**Objections to the Drawings**

In the Office Action mailed July 21, 2005, the drawings were objected to under 37 CFR 1.83(a) for allegedly failing to show every feature of the invention specified in the claims.

In making this objection, the Office Action asserted "the ratio between the gate length and the gate width of one of the transistors in each pair, and the gate voltage capacity of the first to fourth transistors of the level conversion circuit greater than the gate voltage capacity of the first to fourth transistors in the differential amplification circuit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered." Office Action, p. 2.

The Applicants respectfully traverse the objection, as follows. The Applicants submit that the ratio between the gate length and gate width of the transistors is illustrated in Fig. 14, which is a graph showing the relationship between the gate width to length ratio ( $W/L$ ) of the transistors and the delay time  $t_{PD}$  of the input circuit. In

particular, the horizontal axis of the graph of FIG. 14 “represents the ratio  $W/L(M1)$  of the gate length  $L$  and the gate width  $W$  in the first MOS transistor  $M1$  relative to the ratio  $W/L(M2)$  of the gate length  $L$  and the gate width  $W$  in the second MOS transistor  $M2$ .” Application No. 10/809,894, page 26, lines 9-14. The specification goes on to describe the effect on the delay time  $t_{PD}$  of the input circuit for cases in which “the ratio  $W/L(M1)$  of the MOS transistor  $M1$  is equal to the ratio  $W/L(M2)$  of the MOS transistor  $M2$ ,” “the ratio  $W/L(M1)$  is 0.5 times the ratio  $W/L(M2)$ ,” and “the ratio  $W/L(M1)$  becomes greater than the ratio  $W/L(M2)$ ,” even when the levels of the input signals  $IN$  and  $INB$  change. Id., at page 26. The specification further discloses that “it is preferable that the level conversion circuit 11 be designed so that the ratio  $W/L(M1)$  of the MOS transistor  $M1$  is three times or less than the ratio  $W/L(M2)$  of the MOS transistor  $M2$  as shown in FIG. 14.” Id.

Thus, the Applicants submit that the features of “the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors” recited in claims 2, 15 and 18, and “the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors” recited in claims 3 and 19, are fully illustrated and described by the specification at Fig. 14 and the description thereof.

Regarding the gate voltage capacities of the respective transistors, notation has been added to Fig. 5 indicating that the gate voltage capacity of transistors M1-M4 is greater than that of transistors MP1, MP2, MN1 and MN2. In addition, new drawing Figure 15 has been added, illustrating exemplary thicknesses of the gate oxide film of transistors M1-M4 and transistors MP1, MP2, MN1, MN2 of Fig. 5. In addition, the specification has been amended to provide a brief description of new Fig. 15. No new matter has been added, as the subject matter of amended Fig. 5 and new Fig. 15 is fully disclosed in the specification as filed, at, for example, page 13, lines 22-33.

The Applicants submit that the drawings are in compliance with the rules of U.S. patent practice, and withdrawal of the objection is requested.

**Rejection Under 35 USC § 112**

Claim 5 was rejected under 35 U.S.C. § 112, first paragraph. Claim 5 has been amended responsive to this rejection. If any additional amendment is necessary to overcome the objections and rejection, the Examiner is requested to contact the Applicant's undersigned representative.

**Rejections Under 35 USC § 102(e)**

In the outstanding Office Action, claims 1, 3, 4, 6, 15-17, 19 and 20 were rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,590,422 to Dillon ("Dillon"). Claims 2, 7-14 and 18 were objected to as depending from a rejected base claim. It is noted that claims 1 and 17 have been canceled, and claims 2-9, 11-14 and 18-20 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Claims 2, 7-14 and 18 have been amended to be in independent form, including the subject matter of the base claim and any intervening claims. Thus, claims 2, 7-14 and 18 are in condition for allowance. In addition, claims 3, 4 and 6 have been amended to depend from allowable claim 2, and claims 19 and 20 have been amended to depend from allowable claim 18. Thus, claims 3, 4, 6, 19 and 20 are allowable for the same reasons as claim 2 or 18, as well as for the additional subject matter recited therein. Claim 15 has been amended to include the allowable subject matter of claim 2. Thus, claim 15 is allowable for the same reasons as claim 2, as well as for the additional subject matter recited therein.

Applicants respectfully request withdrawal of the rejections and objections in this application.

### **Conclusion**

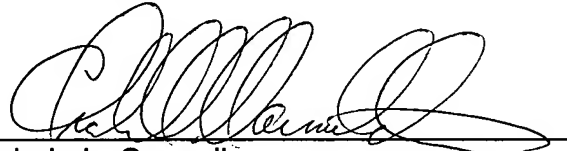
For all of the above reasons, it is respectfully submitted that claims 2-16 and 18-20 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number **108075-00126**.

Respectfully submitted,

Arent Fox, PLLC

A handwritten signature in black ink, appearing to read 'Michele L. Connell', written over a horizontal line.

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Enclosures: Replacement Sheet  
New Sheet